晶 發 科 技 股 份 有 限 公 司
GI FAR TECHNOLOGY CO.,LTD
No. 81, Dongfeng St, Shulin District, 23874, New Taipei City, Taiwan, R.O.C.

SPECIFICATIONS

CUSTOMER : _____

MODEL NO. : GFB248060A-FTNE

VERSION : D

DATE : 2017.04.26

CERTIFICATION : ROHS

CUSTOMER SIGN : _____

QA Approved By	Approved By	Prepared By	Prepared By
	GIFAR 2017.07.25 Donlin	GIFAR 2017.07.25 Hazel	GIFAR 2017.07.25 Rita

晶 發 科 技 股 份 有 限 公 司
GI FAR TECHNOLOGY CO.,LTD
新北市樹林區東豐街 81 號
No. 81, Dongfeng St, Shulin District, 23874, New Taipei City, Taiwan, R.O.C.
TEL: +886-2-8684-1188 FAX: +886-2-8684-8532

Revision Record

Data(y/m/d)	Ver.	Description	Note	page
2012.01.06	A	Specification released		
2012.03.07	B	增加標籤及膠帶		15
2016.08.24	C	增加 PI 膠帶 正面 IC*4+LCD*1，背面板子*1		15
2017.04.26	D	修改公司抬頭、格式統一		

CONTENTS

1. SCOPE

This specification covers the engineering requirements for the GFB248060A-FTNE liquid crystal module.

2. PRODUCT SPECIFICATIONS

2.1 General

- 248 × 60 dot matrix LCD
- FSTN , Positive mode LCD panel
- Transmissive , Wide temperature type
- 6 o'clock
- Multiplexing driving : 1/64 duty, 1/9 bias
- TAB S6B0719x2
- ROHS

2.2 Mechanical Characteristics

Item	Characteristic
Dot configuration	248 × 60
Dot dimensions(mm)	0.38 × 0.34
Dot spacing (mm)	0.03
Module dimensions (Horizontal × Vertical × Thickness, mm)	123 × 97.6 × 2.85 max.
Viewing area (Horizontal × Vertical, mm)	120.2 × 27.1
Active area (Horizontal × Vertical, mm)	94.21 × 20.37

2.3 Absolute Maximum Ratings (Without LED back-light)

(Vss = 0V)

Parameter	Symbol	Rating	Unit
Supply voltage range	VDD	- 0.3 ~ + 7.0	V
	V0, VOUT	+ 0.3 ~ + 17.0	V
	V1, V2, V3, V4	+ 0.3 ~ V0	V
External reference voltage	VEXT	+0.3 ~ VDD	
Input voltage range	VIN	- 0.3 ~ VDD + 0.3	V
Operating temperature range	TOPR	- 40 ~ + 85	°X
Storage temperature range	TSTR	- 55 ~ + 125	°X

NOTES:

1. VDD, V0, VOUT, V1 to V4, VEXT and VCI are based on Vss = 0V.
2. Voltage VOUT ≥ V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS must always be satisfied.
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently.
   It is desirable to use this LSI under electrical characteristic conditions during general operation.
   Otherwise, this LSI may malfunction or reduced LSI reliability may result.

2.4 Electrical Characteristics (Without LED back-light)

DC Characteristics (V_{SS} = 0V, V_{DDI}= 2.4 to 3.6V, Ta = -40~85°C)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Operating voltage (1)		V_{DD}		3.3	-	5	V	V_{DD} *1
Operating voltage (2)		V0		4.0	-	15.0	V	V0, *2
Input voltage	High	V_{IH}		0.8V_{DD}	-	V_{DD}	V	*3
	Low	V_{IL}		V_{SS}	-	0.2V_{DD}		
Output voltage	High	V_{OH}	I_{OH} = -0.5mA	0.8V_{DD}	-	V_{DD}	V	*4
	Low	V_{OL}	I_{OL} = 0.5mA	V_{SS}	-	0.2V_{DD}		
Input leakage current		I_{IL}	V_{IN} = V_{DD} or V_{SS}	- 1.0	-	+ 1.0	μA	*3
Output leakage current		I_{OZ}	V_{IN} = V_{DD} or V_{SS}	- 3.0	-	+ 3.0	μA	*5
LCD driver ON resistance		R_{ON}	Ta = 25°C, V0 = 8V	-	2.0	3.0	kΩ	SEGn COMn *6
Frame frequency		f_{FR}	Ta = 25°C	70	85	100	Hz	*7 FR

DC Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Voltage converter circuit output voltage	VOUT	×3 / ×4 / ×5 / ×6 voltage conversion (no-load)	95	99	-	%	VOUT
Voltage regulator circuit operating voltage	VOUT		6.0	-	17.0	V	VOUT
Voltage follower circuit operating voltage	V0		4.0	-	15.0	V	V0 *8
Reference voltage	V_{REF}	Ta = 25°C	1.94	2.00	2.06	V	*9

2.5 Optical Characteristics Absolute maximum ratings

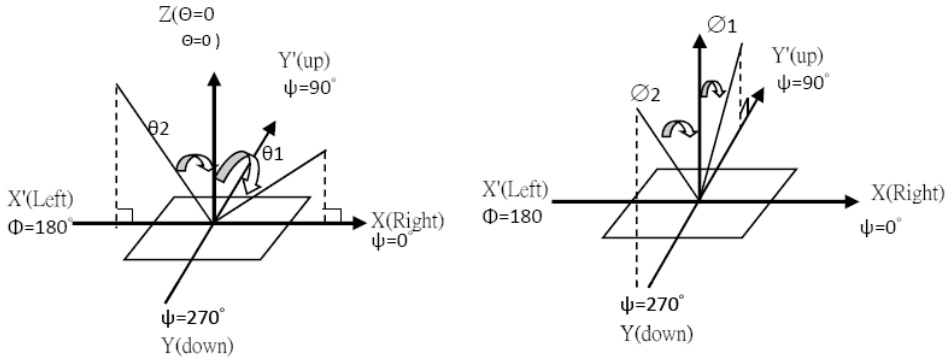
Item	Symbol	Rating	Unit
Operating temperature range	Top	-20~70	°C
Storage temperature range	Tst	-40~80	°C

2.6 Optical Characteristics

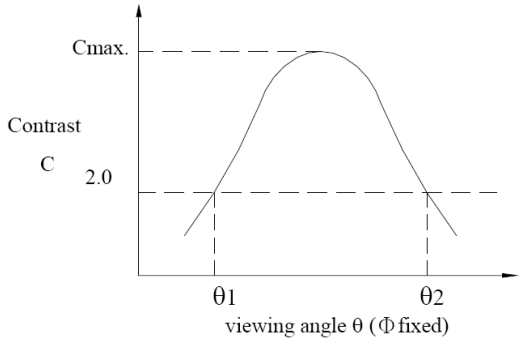
1/64 duty, 1/9bias, Vop=13.2v,Ta=25°C

Item	Symbol	Conditions	Min.	Typ.	Max	Reference
Driving voltage	Vop	25 °C	--	13.2	--	
Viewing angle	θ	C≥2.0,∅=0° C	30°	--	--	Notes 1 & 2
Contrast	C	θ=5°, ∅=0°	2.0	--	--	Note 3
Response time(rise)	tr	θ=5°, ∅=0°	--	--	TBD	Note 4
Response time(fall)	tf	θ=5°, ∅=0°	--	--	TBD	Note 4

Note 1: Definition of angles θ and ∅

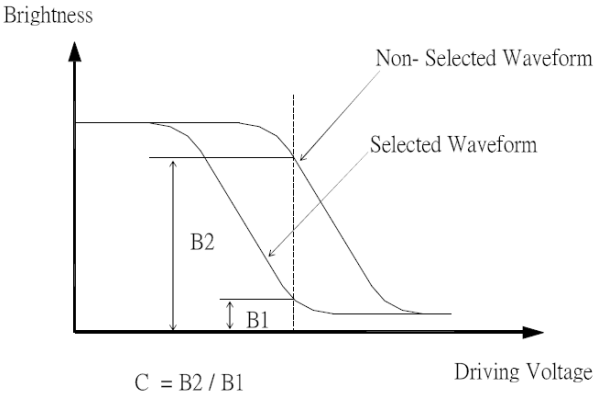


Note 2: Definition of viewing angles θ1 and θ2



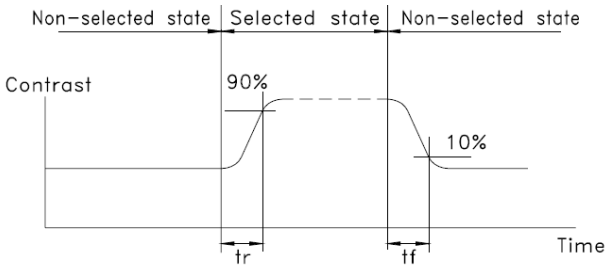
Note : Optimum viewing angle with the naked eye and viewing angle θ at Cmax. Above are not always the same

Note 3: Definition of contrast C



C = B2 / B1

Note 4: Definition of response time



Note: Measured with a transmissive LCD panel which is displayed 1 cm^2

V_{OPR} : Operating voltage f_{FRM} : Frame frequency
t_{ON} : Response time (rise) t_{OFF} : Response time (fall)

3. RELIABILITY

NO.	ITEM	CONDITION		STANDARD	NOTE
1	High Temp. Storage	80℃	120 hrs	Appearance Without defect	
2	Low Temp. Storage	-40℃	120 hrs	Appearance Without defect	
3	High Temp. & High Humi. Storage	40℃ 90% RH	120 hrs	Appearance Without defect	
4	High Temp. Operating Display	70℃	120 hrs	Appearance Without defect	
5	Low Temp. Operating Display	-20℃	120 hrs	Appearance Without defect	
6	Thermal Shock	-20℃, 30min. → 70℃,30min. (1cycle)		Appearance Without defect	10 cycles

** Dissipation current, contrast and display functions
** Polarizing filter deterioration, other appearance defects
** The function test shall be conducted after 4hours storage at the normal temperature and humidity after remove from the test chamber.

4. OPERATING INSTRUCTIONS

4.1 Input signal Function

<table>
<tr><th>NO.</th><th>Symbol</th><th>Function</th></tr>
<tr><td>1</td><td>VSS</td><td>Ground</td></tr>
<tr><td>2</td><td>NC</td><td>NC</td></tr>
<tr><td>3</td><td>VDD</td><td>Power supply for logic</td></tr>
<tr><td>4-11</td><td>D7-D0</td><td>8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data
bus. When the serial interface selected (PS = "L");
DB0 to DB5: high impedance
DB6: serial input clock (SCLK)
DB7: serial input data (SID).
When chip select is not active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>12</td><td>RESETB</td><td>Reset input pin
When RESETB is “L”, initialization is executed.</td></tr>
<tr><td>13</td><td>SCL</td><td>serial input clock(PCB SDI_R Short)</td></tr>
<tr><td>14</td><td>SI</td><td>serial input data (PCB SCL_R Short)</td></tr>
<tr><td>15</td><td>PS</td><td>Parallel / Serial data input select input
<table>
<tr><th>PS</th><th>Interface mode</th><th>Data / instruction</th><th>Data</th><th>Read / Write</th><th>Serial clock</th></tr>
<tr><td>H</td><td>Parallel</td><td>RS</td><td>DB0 to DB7</td><td>E_RD
RW_WR</td><td>-</td></tr>
<tr><td>L</td><td>Serial</td><td>RS</td><td>SID (DB7)</td><td>Write only</td><td>SCLK (DB6)</td></tr>
</table>
*NOTE: When PS is “L”, DB0 to DB5 are high impedance and E_RD and RW_WR must be fixed to either “H” or “L”.</td></tr>
<tr><td>16</td><td>CS1B</td><td rowspan="2">Chip select input pins
Data / instruction I/O is enabled only when CS1B is “L”(Master) ,CS2B is “L”(Slave).
When chip select is non-active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>17</td><td>CS2B</td></tr>
<tr><td>18</td><td>RS</td><td>Register select input pin
RS = "H": DB0 to DB7 are display data.
RS = "L": DB0 to DB7 are control data.</td></tr>
<tr><td>19</td><td>WR</td><td>Read/Write execution control pin</td></tr>
<tr><td>20</td><td>RD</td><td>Read/Write execution control pin</td></tr>
<tr><td>21</td><td>PAD1</td><td>User Define</td></tr>
<tr><td>22</td><td>PAD2</td><td>User Define</td></tr>
</table>

Parallel / Serial Interface Mode

PS	Type	CS1B	CS2B	C68	Interface mode
H	Parallel	CS1B	CS2B	H(PCB_R7)	6800-series MPU mode Default 8080 Mode
				L(PCB_R8)	8080-series MPU mode Default 8080 Mode
L	Serial	CS1B	CS2B	--	Serial-mode

4.2 Voltage Converter Circuit

[C1 = 1.0 to 4.7 μF]

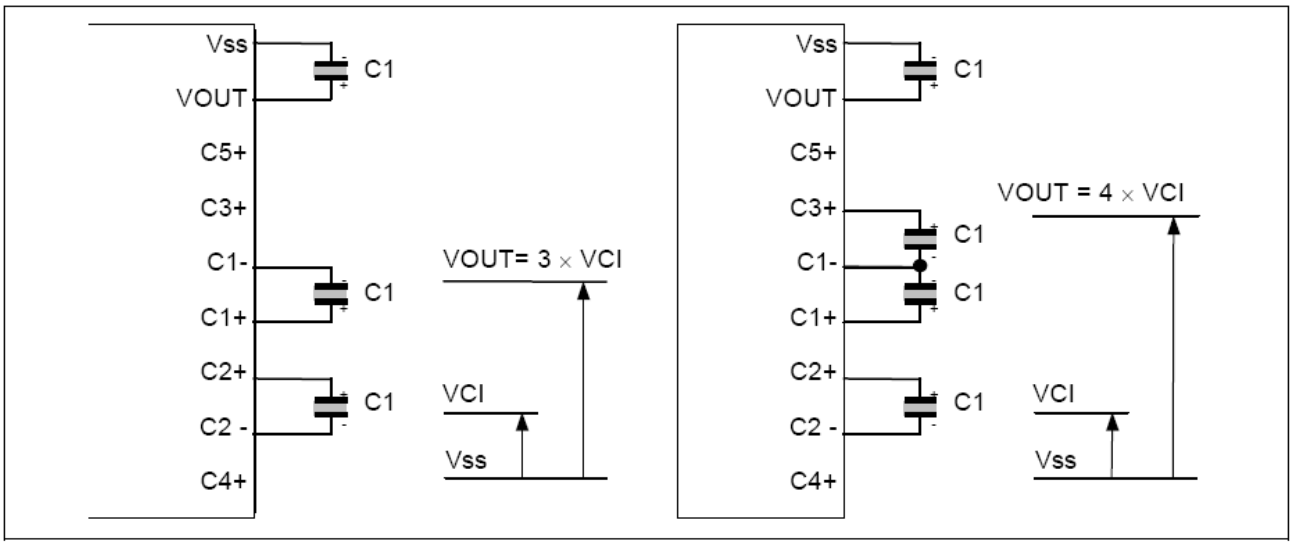


Figure 15. Three Times Boosting Circuit

Figure 16. Four Times Boosting Circuit

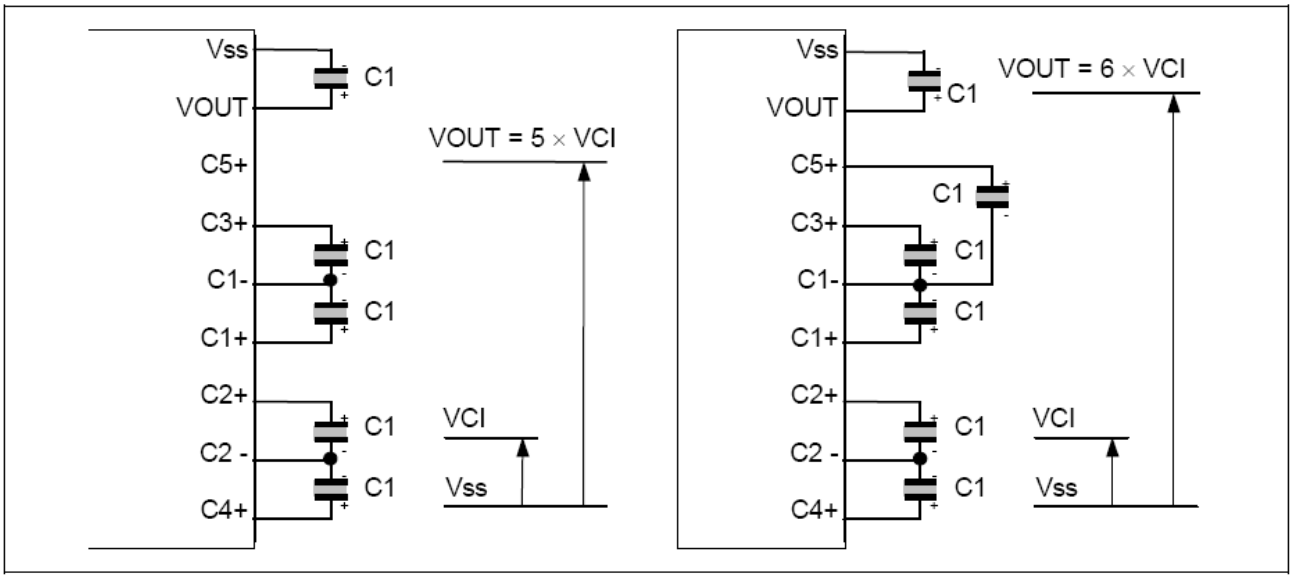


Figure 17. Five Times Boosting Circuit

Figure 18. Six Times Boosting Circuit

MICROPROCESSOR INTERFACE

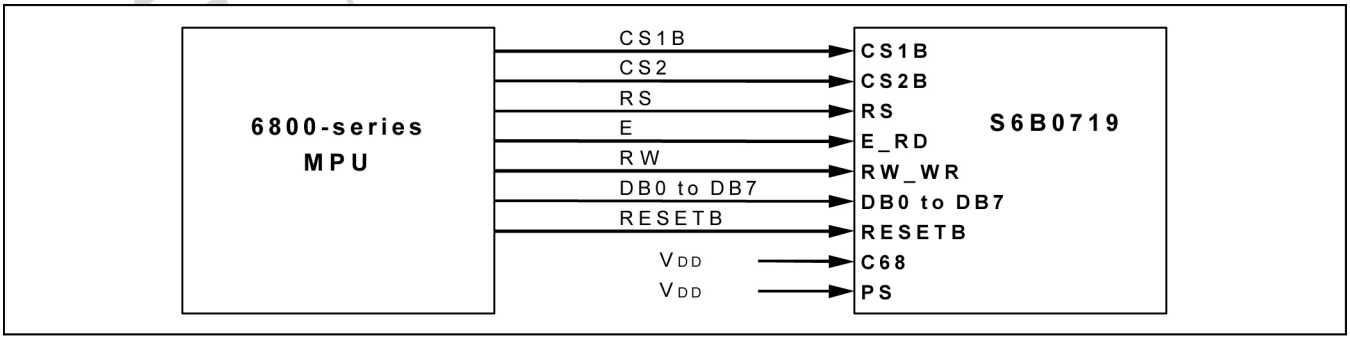


Figure 43. In Case of Interfacing with 6800-series (PS = “H”, C68 = “H”)

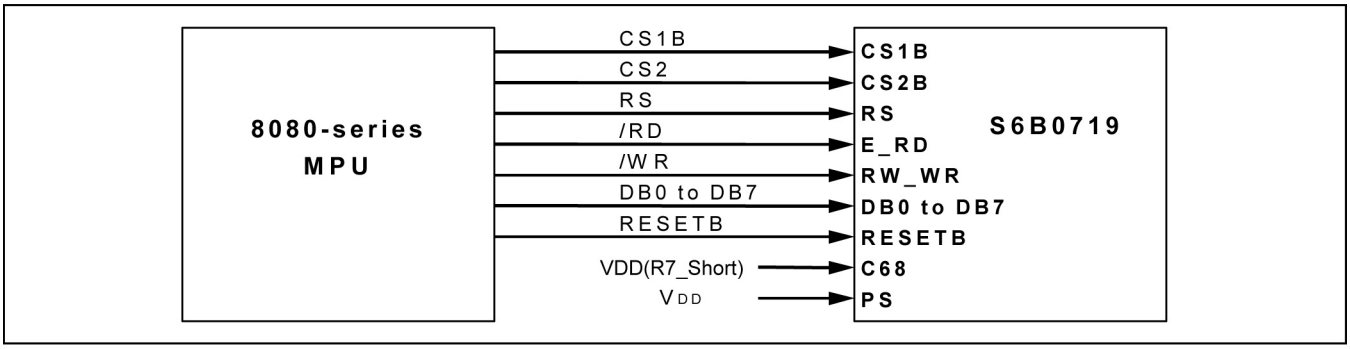


Figure 44. In Case of Interfacing with 8080-series (PS = “H”, C68 = “L”)

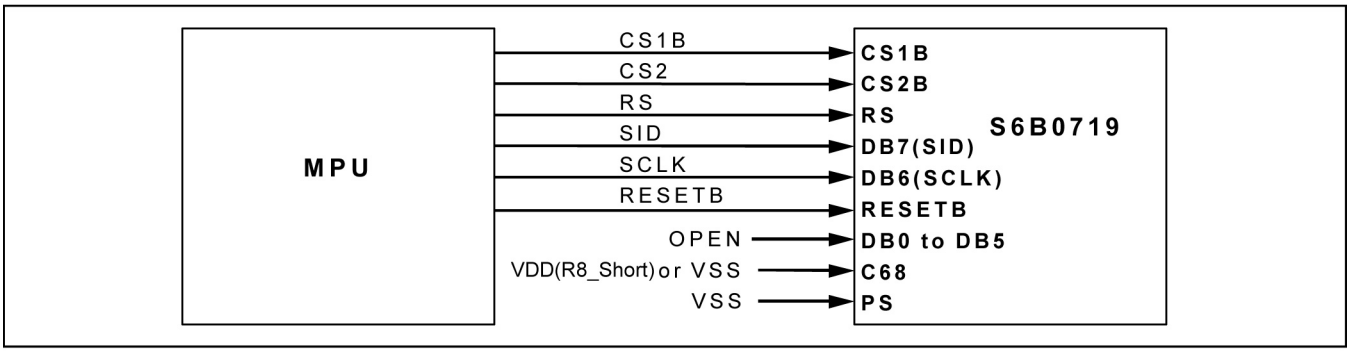


Figure 45. In Case of Serial Interface (PS = “L”, C68 = “H/L”)

4.3 Timing Diagram

Read / Write Characteristics (8080-series MPU)

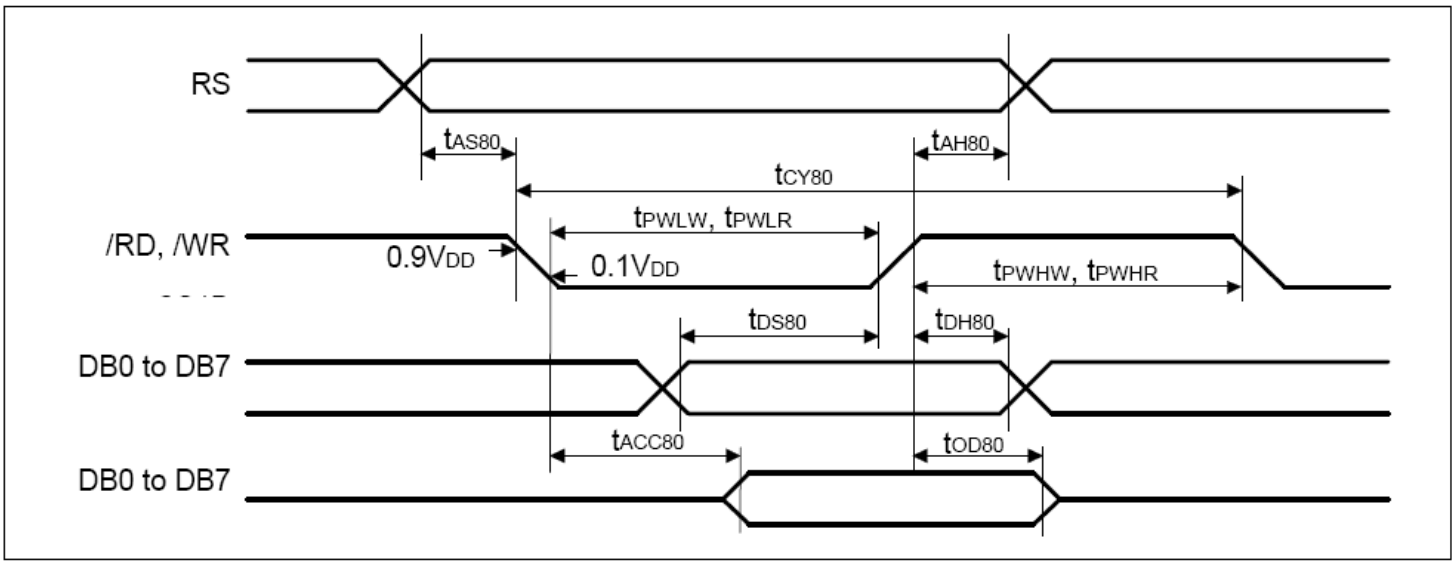


Figure 39. Parallel Interface (8080-series MPU) Timing Diagram

Table 27. AC Characteristics (8080-series Parallel Mode)

(V_{DDI} = 2.4 ~ 3.6V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time Address hold time	RS	t_{AS80} t_{AH80}		0 0	- -	ns
System cycle time		t_{CY80}		300	-	ns
Pulse width low for write Pulse width High for write	RW_WR (/WR)	t_{PWLW} t_{PWHW}		60 60	- -	ns
Pulse width low for read Pulse width high for read	E_RD (/RD)	t_{PWLR} t_{PWHR}		120 60	- -	ns
Data setup time Data hold time	DB0 to DB7	t_{DS80} t_{DH80}		40 15	- -	ns
Read access time Output disable time		t_{ACC80} t_{OD80}	CL = 100 pF	- 10	140 100	ns

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(tr + tf) < (tCY80 - tPWLW - tPWHW) for write, (tr + tf) < (tCY80 - tPWLR - tPWHR) for read

Read / Write Characteristics (6800-series Microprocessor)

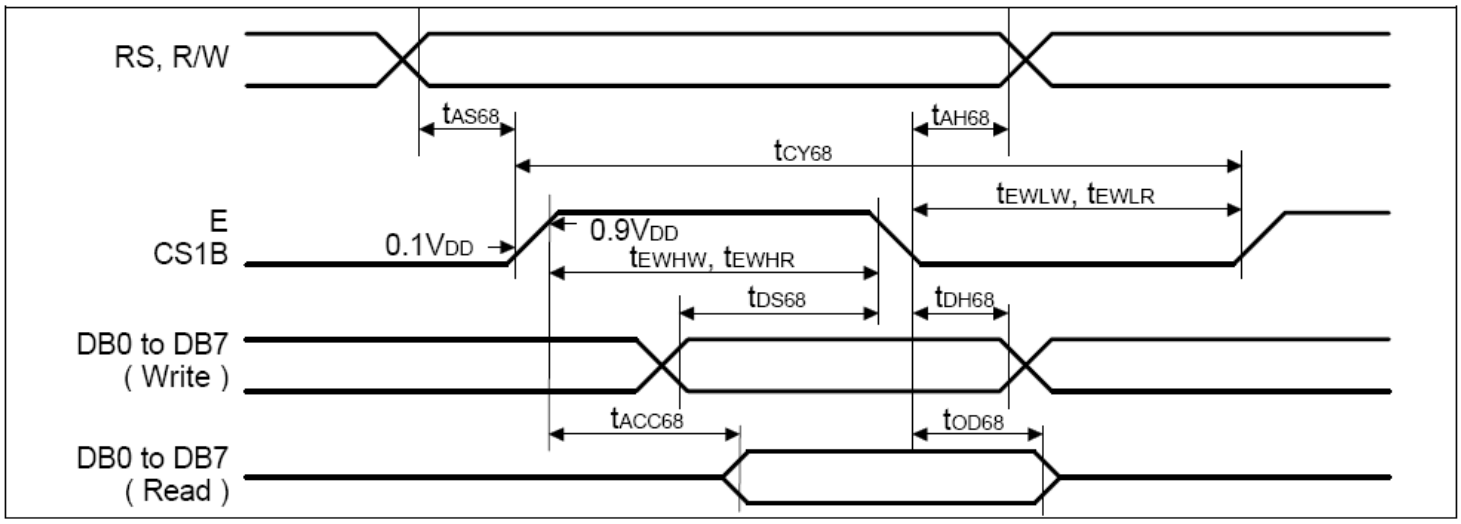


Figure 40. Parallel Interface (6800-series MPU) Timing Diagram

Table 28. AC Characteristics (6800-series Parallel Mode)

(V_{DDI} = 2.4 ~ 3.6V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time Address hold time	RS RW	t_{AS68} t_{AH68}		0 0	- -	ns
System cycle time		t_{CY68}		300	-	ns
Enable width high for write Enable width low for write	E_RD (E)	t_{EWHW} t_{EWLW}		60 60	- -	ns
Enable width high for read Enable width low for read	E_RD (E)	t_{EWHR} t_{EWLR}		120 60	- -	ns
Data setup time Data hold time	DB0 to DB7	t_{DS68} t_{DH68}		40 15	- -	ns
Read access time Output disable time		t_{ACC68} t_{OD68}	C_L = 100 pF	- 10	140 100	ns

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(tr + tf) < (tCY68 - tEWHW - tEWLW) for write, (tr + tf) < (tCY68 - tEWHR - tEWLR) for read

Serial Interface Characteristics

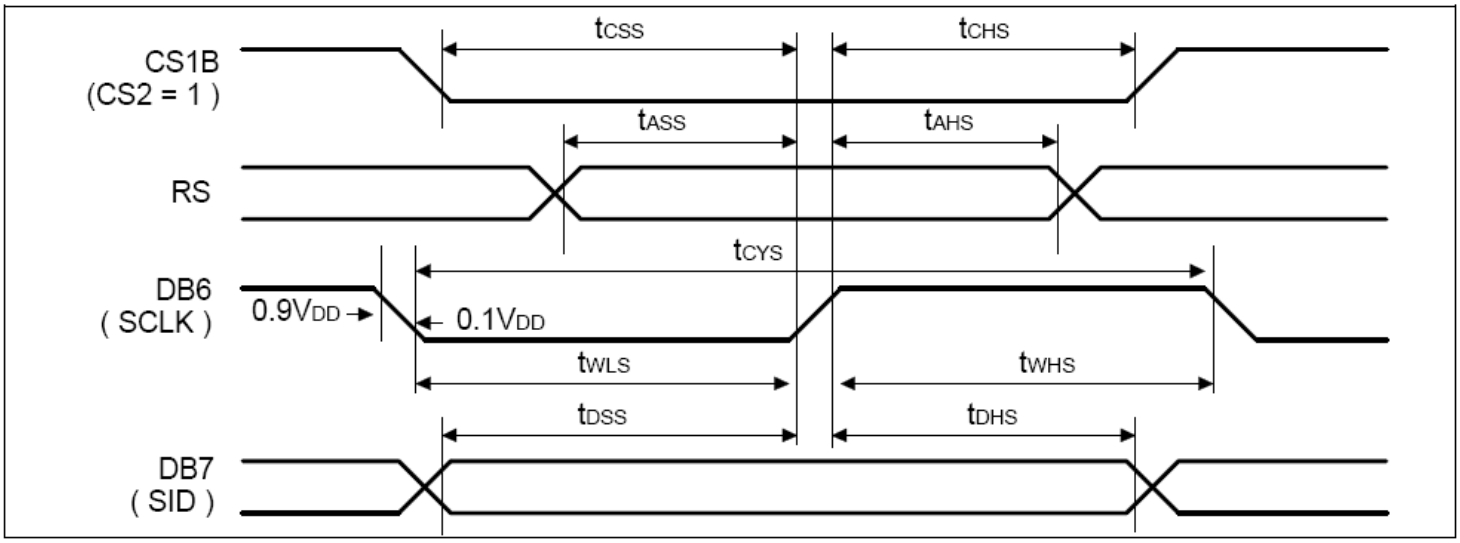


Figure 41. Serial Interface Timing Diagram

Table 29. AC Characteristics (Serial Mode)

(V_{DDI} = 2.4 ~ 3.6V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	t_{SCY} t_{SHW} t_{SLW}		250 100 100	- - -	ns
Address setup time Address hold time	RS	t_{ASS} t_{AHS}		150 150	- -	ns
Data setup time Data hold time	DB7 (SID)	t_{DSS} t_{DHS}		100 100	- -	ns
CS1B setup time CS1B hold time	CS1B	t_{CSS} t_{CHS}		150 150	- -	ns

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

5. NOTES

Safety

- If the LCD panel breaks, be careful not to get the liquid crystal in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

Handling

- Avoid static electricity as this can damage the CMOS LSI.
- The LCD panel is plate glass; do not hit or crush it.
- Do not remove the panel or frame from the module.
- The polarizing plate of the display is very fragile; handle it very carefully

Mounting and Design

- Mount the module by using the specified mounting part and holes.
- To protect the module from external pressure, leave a small gap by placing transparent plates (e.g. acrylic or glass) on the display surface, frame, and polarizing plate
- Design the system so that no input signal is given unless the power-supply voltage is applied.
- Keep the module dry. Avoid condensation, otherwise the transparent electrodes may break.

Storage

- Store the module in a dark place where the temperature is 25 ºC±10 ºC and the humidity below 65% RH.
- Do not store the module near organic solvents or corrosive gases.
- Do not crush, shake, or jolt the module (including accessories).

Cleaning

- Do not wipe the polarizing plate with a dry cloth, as it may scratch the surface.
- Wipe the module gently with soft cloth soaked with a petroleum benzine.
- Do not use ketonic solvents (ketone and acetoe) or aromatic solvents (toluene and xylene), as they may damage the polarizing plate.

6. OPERATION PRECAUTIONS

Any changes that need to be made in this specification or any problems arising from it will be dealt with quickly by discussion between both companies.

7. LCM Dimension