SPECIFICATIONS

CUSTOMER : _____

MODEL NO. : TES-GFDBP18F46K22A

VERSION : B

DATE : 2019.03.06

CERTIFICATION : ROHS

Customer Sign	Approved By	Prepared By	Prepared By
	GIFAR 2019.03.06 Sidney	GIFAR 2019.03.06 Hazel	GIFAR 2019.03.06 Rita

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Revision Record

Data(y/m/d)	Ver.	Description	Note	page
2015.01.06	A	New		
2019.03.06	B	修改公司抬頭、格式統一		

CONTENTS

General Description:

This_Demoboard is a LCM control board for Mono Display or MCU TFT.

1. Features:

High Performance RISC CPU: PIC18F46K22

- C Compiler optimized architecture/instruction set
- Data EEPROM to 1024 bytes
- Linear program memory addressing to 64 Kbytes
- Linear data memory addressing to 4 Kbytes
- Up to 16 MIPS operation
- 16-bit wide instructions, 8-bit wide data path
- Priority levels for interrupts
- 31-level, software accessible hardware stack
- 8 x 8 Single-Cycle Hardware Multiplier

2 LCD output Interface (2PIN,1ZIF) →8bit*2 + 8*2Bit*1

Drive 2sets LCM at the same time, easy to do comparison
→M26PA||M26PB

With LED driving circuit, control Backlight with fix forward current
→LEDA||LEDK(Option)

DC power supply(outside) : 9V / 1A →J1

LCM Voltage output: 3.3V or 5.0V (optional) →JP1

3 Bottoms (for test function) →SW1||SW2||SW3

ICSP burn through ICD →ICSP

2. Electrical specification

2.1 Absolute max. Ratings

Electrical Absolute max. ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	J1 Power	VSS=0	-0.3	15	V	

2.2 Electrical characteristics

DC Electrical characteristic of the control Board

Typical operating conditions (VSS=0V)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
External Power supply	PVDD	7.5	9	12	V	Note 1

3. Interface specifications

3.1 M26PA

Pin no	Symbol	I/O	Description	Remark
1	VCC	I	JP1 SEL	
2	GND	I	Ground	
3	RS/A0	I/O	Indicates that D0 to D7 are display data or control data..	PORTAbits.RA0
4	VOA	O	Contrast voltage, ADJ By VRA1	
5	/RD(E)	I/O	/RD Control	PORTAbits.RA1
6	/WR	I/O	/WR Control	PORTAbits.RA2
7	D1	I/O	Data Bus	PORTBbits.RB1
8	D0	I/O	Data Bus	PORTBbits.RB0
9	D3	I/O	Data Bus	PORTBbits.RB3
10	D2	I/O	Data Bus	PORTBbits.RB2
11	D5	I/O	Data Bus	PORTBbits.RB5
12	D4	I/O	Data Bus	PORTBbits.RB4
13	D7	I/O	Data Bus	PORTBbits.RB7
14	D6	I/O	Data Bus	PORTBbits.RB6
15	TX	I/O	Data Bus	PORTCbits.RC6
16	RX	I/O	Data Bus	PORTCbits.RC7
17	CS	I/O	Master/Slave SPI Input/Output	PORTAbits.RA3
18	DATA	I/O	Master/Slave SPI Input/Output	PORTCbits.RC5
19	CLK	I/O	Master/Slave SPI Input/Output	PORTCbits.RC3
20	/CS	I/O	Chip Select Control	PORTAbits.RA3
21	/CS	I/O	Chip Select Control	PORTAbits.RA3
22	/RST	I/O	The reset operation is performed by the /RES signal level.	PORTAbits.RA4
23	GPIO5	I/O	GPIO	PORTCbits.RC5
24	VEEA	I	External voltage input to provide LCD VOP	
25	LEDK	O	Backlight LEDK(-)	
26	LEDAA	O	Backlight LEDA(+)	

3.2 S1(Power Switch)

Pin no	Symbol
1	Short /Power ON
2	Open /Power OFF

3.3 JP1

JP1(1,2)	VDD5V
JP1(2,3)	VDD3.3V

3.4 ICSP

Pin no	Symbol
1	VPP
2	VCC
3	GND
4	ICDDAT
5	ICDCLK
6	NC

3.5 MCU_TFT for Gifar MCU Series

Pin no	Symbol	Pin no	Symbol	Pin no	Symbol	Pin no	Symbol
1	GND	11	D13	21	D3	31	NC
2	VCC	12	D12	22	D2	32	LEDK
3	/WR	13	D11	23	D1	33	LEDAA
4	/RD	14	D10	24	D0		
5	/CS	15	D9	25	CNF A		
6	NC	16	D8	26	GPIO0		
7	/RST	17	D7	27	GPIO1		
8	RS	18	D6	28	GPIO2		
9	D15	19	D5	29	GPIO3		
10	D14	20	D4	30	GPIO4		

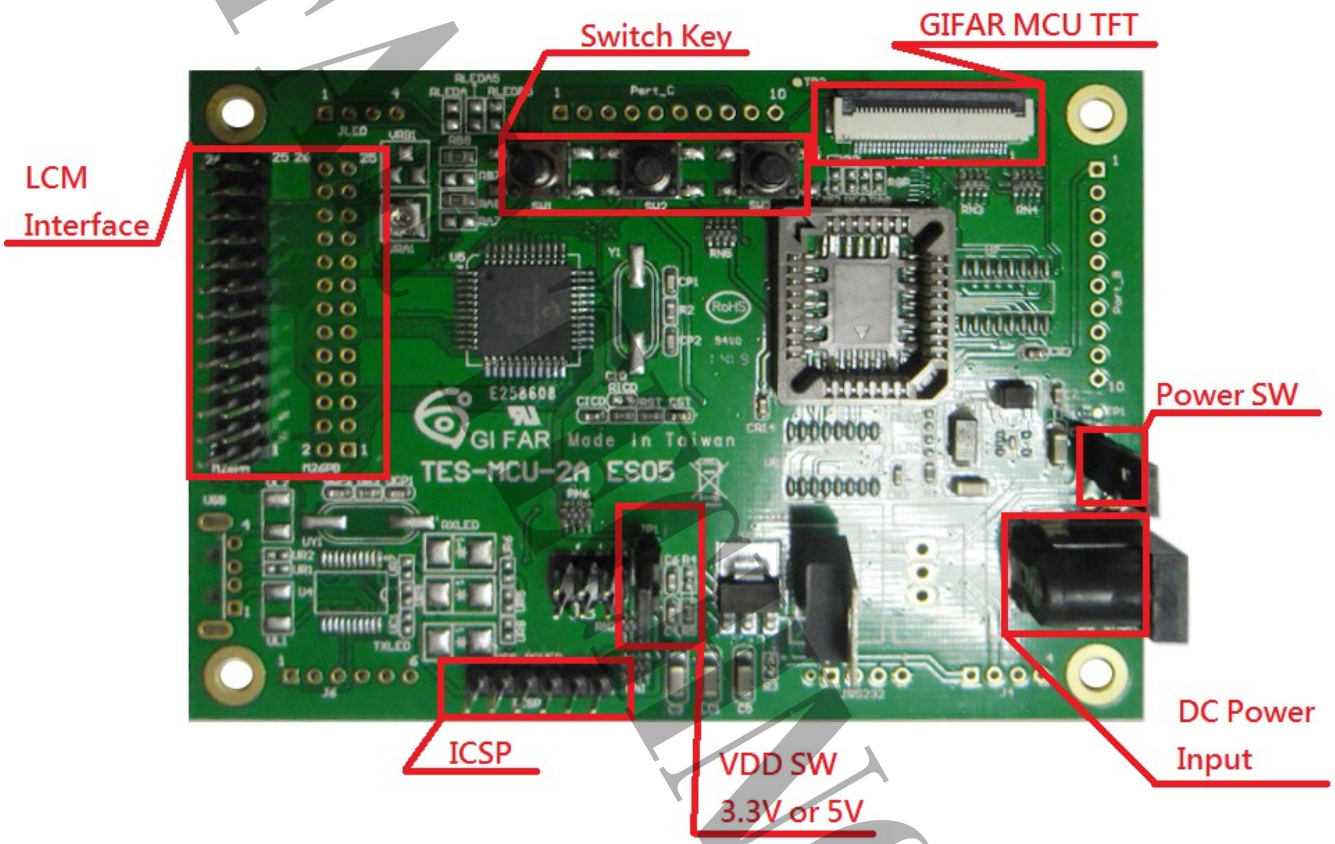
3.6 J3

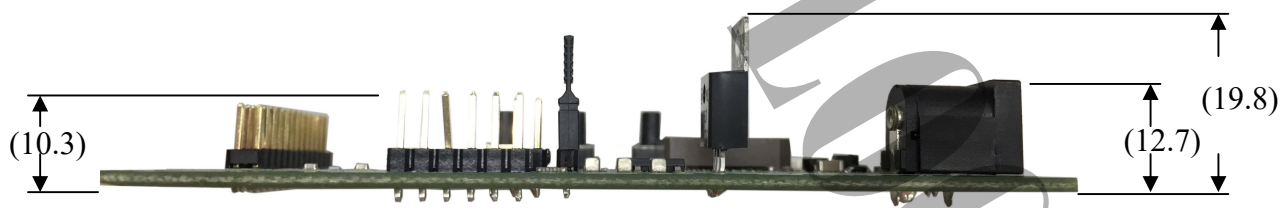
JP3(1,2)	SW1
JP3(3,4)	SW2
JP3(5,6)	SW3

3.7 DC JACK

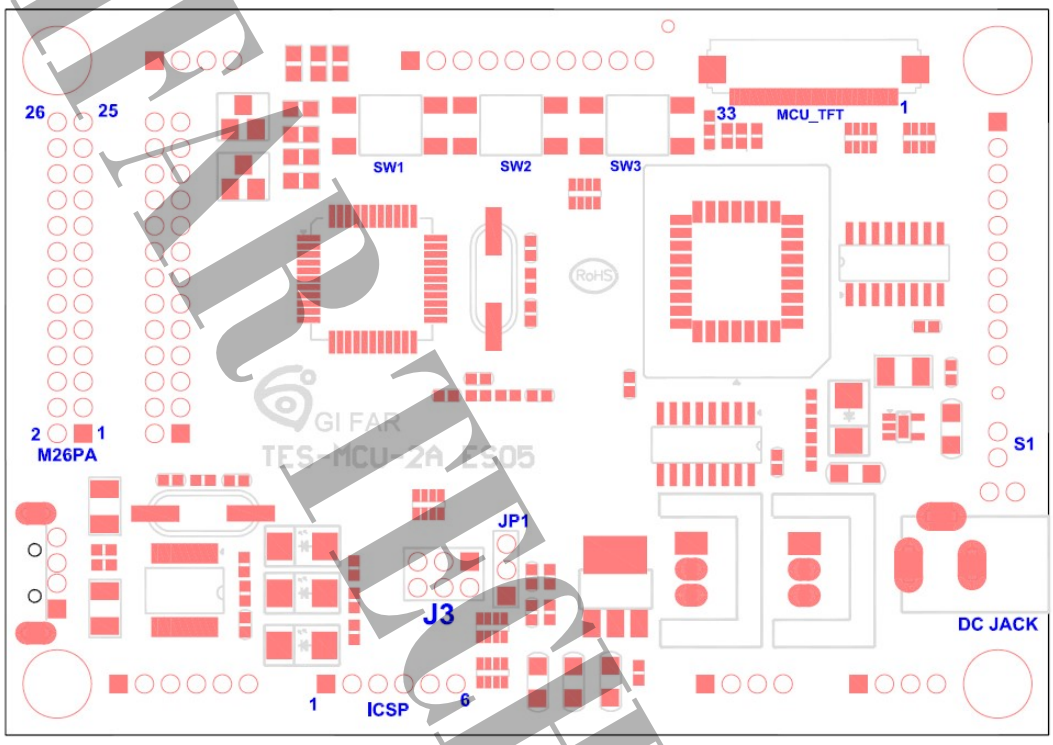
DC9V φ2.0mm

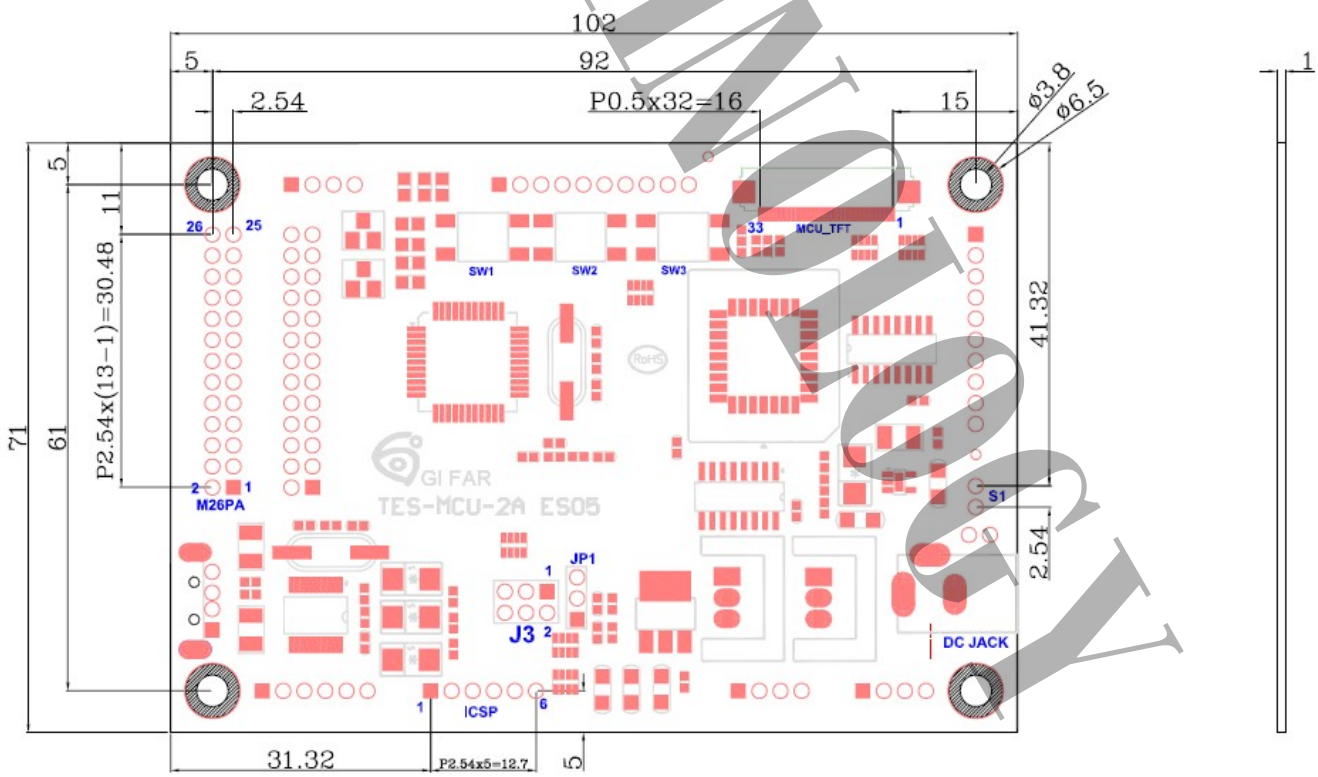
4. Block Diagram





5. PCB Drawing





6. Schematic